ABSTRACT

[0090] A system and method are disclosed which enable resolution of conflicts between memory access requests in a manner that allows for efficient usage of cache memory. In one embodiment, a circuit comprises a cache memory structure comprising multiple banks, and a plurality of access ports communicatively coupled to such cache memory structure. The circuit further comprises circuitry operable to determine a bank conflict for pending access requests for the cache memory structure, and circuitry operable to issue at least one access request to the cache memory structure out of the order in which it was requested, responsive to determination of a bank conflict.